REMARKS/ARGUMENTS

Claims 10-27 are rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter. Claims 1-8, 10-17, and 19-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen (US Patent No. 5,751,614). Claims 1-18 and 28-41 are pending. Claims 10-18 have been amended, and new claims 28-41 have been added.

Rejections under 35 U.S.C. § 101

Regarding the non-statutory subject matter rejections, claims 10-18 have been amended, and claims 19-27 have been cancelled. As amended, claims 10-18 are believed to overcome the non-statutory subject matter rejections. Support for this amendment can be found, for example, in paragraph [0079] of the published application.

Rejections under 35 U.S.C. § 103

Regarding the obviousness rejections, the Cohen reference cited by the Examiner fails to qualify as prior art to the pending claims. The present application claims priority back to the 8/16/95 filing date of U.S. Patent Application No. 08/516,036, which issued into U.S. Patent No. 5,742,840 (the '840 patent). This chain of priority also includes a continuation-in-part application, U.S. Patent Application No. 09/382,402, which issued into U.S. Patent no. 6,295,599 (the '599 patent). The priority claim is hereby reproduced for the convenience of the Examiner:

> This application is a continuation of U.S. patent application Ser. No. 10/646,787, filed Aug. 25, 2003, which is a continuation of U.S. patent application Ser. No. 09/922,319, filed Aug. 2, 2001, which is a continuation of U.S. patent application Ser. No. 09/382,402, filed Aug. 24, 1999, now U.S. Pat. No. 6,295,599, which claims the benefit of priority to Provisional Application No. 60/097,635 filed Aug. 24, 1998, and is a continuation-in-part of U.S. patent application Ser. No. 09/169,963, filed Oct. 13, 1998, now U.S. Pat. No. 6,006,318, which is a continuation of U.S. patent application Ser. No. 08/754,827, filed Nov. 22, 1996 now U.S. Pat. No. 5,822,603, which is a divisional of U.S. patent application Ser. No. 08/516,036, filed Aug. 16, 1995 now U.S. Pat. No. 5,742,840.

Cohen fails to qualify as prior art because the earliest filing date of Cohen associated with the feature cited by the Examiner is 2/29/96. The Examiner cites to the "mask" feature in Fig. 3

of Cohen. Cohen is a continuation-in-part (CIP) of parent application 08/444,814, filed 5/18/95. However, the "mask" feature cited by the Examiner was not disclosed in the parent application. That is, the "mask" feature appeared for the first time in the Cohen application filed 2/29/96, which is after the 8/16/95 priority date of the present application. As such, Cohen fails to qualify as prior art against the pending claims.

All of the obviousness rejections rely on Cohen, which fails to qualify as prior art against the pending claims. As such, the obviousness rejections cannot stand, and claims 1-8 and 10-17 are patentable over the cited reference.

Support for Pending Claims 1-18

As mentioned above, the priority date of 8/16/95 of the present application is established through a claim of priority that includes the '840 patent and its appendix (the '840 appendix) and the '599 patent and its appendix (the '599 appendix). Support for pending claims 1-18 as found in the '840 patent, '840 appendix, '599 patent, and the '599 appendix is presented below.

Regarding claim 1, the recited method for processing data using a programmable processor comprising "decoding a single instruction for writing data to memory specifying both a mask and a register containing data, the mask comprising fields that each correspond to a field of the data contained in the register; detecting some of the fields of the mask as having a predetermined value and identifying corresponding fields of the data contained in the register as write-enabled data fields; and writing the write-enabled data fields to a specified memory location" is described in the '599 patent at Fig. 1 and col. 4, lines 10-66, the '599 appendix at p. 123-25 and 128-30, the '840 patent at Figures 6 and 7, and col. 11, line 19 through col. 13, line 11, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 2, the recited claim feature "wherein each of the fields of the mask has a width of one bit" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 3, the recited claim feature "wherein each of the fields of the data contained in the register has a width of one bit" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 4, the recited claim feature "wherein the writing step further comprises reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled data fields to the specified memory location" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 5, the recited claim feature "wherein the mask is contained in a specified register" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 6, the recited claim feature "wherein the memory location is contained in a specified register" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 7, the recited claim feature "wherein the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 8, the recited claim feature "wherein the predetermined value is a logic 1" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 9, the recited claim feature "further comprising: decoding a second single instruction specifying a third and a fourth register each containing a plurality of floating-point operands; multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality or products; and providing the plurality of products to partitioned fields of a result register as a catenated result" is described in the '599 patent at Fig. 1 and col. 4, lines 10-66, the '599 appendix at p. 258-60, the '840 patent at Figures 6 and 7, and col. 11, line 19 through col. 13, line 11, and the '840 appendix at p. 129-31.

Regarding claim 10, the recited computer-readable medium "having instructions that instruct a computer system to perform operations, at least some of the instructions including a store multiplex instruction for selectively storing data in a programmable processor, the store multiplex instruction capable of instructing a computer to perform operations comprising:

decoding the store multiplex instruction specifying both a mask and a register containing data, the mask comprising fields that each correspond to a field of the data contained in the register; detecting some of the fields of the mask as having a predetermined value and identifying corresponding fields of the data contained in the register as write-enabled data fields; and writing the write-enabled data fields to a specified memory location" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 11, the recited claim feature "wherein each of the fields of the mask has a width of one bit" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 12, the recited claim feature "wherein each of the fields of the data contained in the register has a width of one bit" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 13, the recited claim feature "wherein the writing step further comprises reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled data fields to the specified memory location" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 14, the recited claim feature "wherein the mask is contained in a specified register" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 15, the recited claim feature "wherein the memory location is contained in a specified register" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 16, the recited claim feature "wherein the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 17, the recited claim feature "wherein the predetermined value is a logic 1" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 18, the recited claim feature "wherein at least some of the instructions further include a group floating point multiply instruction for multiplying floating point data in a programmable processor, the group floating point multiply instruction capable of instructing the computer to perform operations comprising: decoding the group floating point multiply instruction specifying a third and a fourth register each containing a plurality of floating-point operands; multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality or products; and providing the plurality of products to partitioned fields of a result register as a catenated result" is described in the '599 appendix at p. 258-60, and the '840 appendix at p. 129-31.

Support for New Claims 28-41

New claims 28-41 are fully supported by the present specification. Support for specific claim elements is identified below by citing to the present specification as published (United States Patent Publication Number US2004/0205325).

Regarding claim 28, the recited method for processing data comprising "decoding a single instruction for performing a bitwise insert operation on data in registers in a register file within the programmable processor, the bitwise insert operation operating on a first operand and a second operand stored in registers in the register file; and for each bit in the first operand, the bitwise insert operation inserting the bit into a corresponding bit position in a destination value if a corresponding bit in the second operand has a first predetermined value" is supported at Figures 52A-C and 53A-C, and paragraphs 0314-18.

Regarding claim 29, the recited claim feature "wherein the first predetermined value is a logic 1" is supported at Figures 52A-C and 53A-C, and paragraphs 0314-18.

Regarding claim 30, the recited claim feature "wherein for each bit in the first operand, a corresponding bit position in the destination value is maintained as unchanged if a corresponding

bit in the second operand has a second predetermined value" is supported at Figures 52A-C and 53A-C, and paragraphs 0314-18.

Regarding claim 31, the recited claim feature "wherein the second predetermined value is a logic 0" is supported at Figures 52A-C and 53A-C, and paragraphs 0314-18.

Regarding claim 32, the recited claim feature "further comprising a step of storing the destination value into memory" is supported at Figures 52A-C and 53A-C, and paragraphs 0314-18.

Regarding claim 33, the recited claim feature "wherein each of the first and second operands has a width of 64 bits" is supported at Figures 52A-C and 53A-C, and paragraphs 0314-18.

Regarding claim 34, the recited claim feature "further comprising a step of executing a plurality of different group floating-point arithmetic operations that arithmetically operate on multiple floating-point operands stored in partitioned fields of an operand register in the plurality of registers to produce a catenated result that is returned to a register in the plurality of registers, wherein the catenated result comprises a plurality of individual floating-point results" is supported at Figures 38A-C and 39A-C, and paragraphs 0235-36.

Regarding claim 35, the recited computer-readable storage medium having stored therein a plurality of instructions comprising "an instruction that causes the processor to perform a bitwise insert operation on data in registers in a register file within the programmable processor, the bitwise insert operation operating on a first operand and a second operand stored in registers in the register file; and wherein for each bit in the first operand, the bitwise insert operation inserts the bit into a corresponding bit position in a destination value if a corresponding bit in the second operand has a first predetermined value" is supported at Figures 52A-C and 53A-C, and paragraphs 0314-18.

Regarding claim 36, the recited claim feature "wherein the first predetermined value is a logic 1" is supported at Figures 52A-C and 53A-C, and paragraphs 0314-18.

Regarding claim 37, the recited claim feature "wherein for each bit in the first operand, a corresponding bit position in the destination value is maintained as unchanged if a corresponding

bit in the second operand has a second predetermined value" is supported at Figures 52A-C and 53A-C, and paragraphs 0314-18.

Regarding claim 38, the recited claim feature "wherein the second predetermined value is a logic 0" is supported at Figures 52A-C and 53A-C, and paragraphs 0314-18.

Regarding claim 39, the recited claim feature "further comprising a step of storing the destination value into memory" is supported at Figures 52A-C and 53A-C, and paragraphs 0314-18.

Regarding claim 40, the recited claim feature "wherein each of the first and second operands has a width of 64 bits" is supported at Figures 52A-C and 53A-C, and paragraphs 0314-18.

Regarding claim 41, the recited claim feature "wherein the plurality of instructions further comprises a plurality of different group floating-point arithmetic operations that arithmetically operate on multiple floating-point operands stored in partitioned fields of an operand register in the plurality of registers to produce a catenated result that is returned to a register in the plurality of registers, wherein the catenated result comprises a plurality of individual floating-point results" is supported at Figures 38A-C and 39A-C, and paragraphs 0235-36.

CONCLUSION

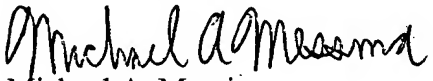
In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Michael A. Messina
Registration No. 33,424

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MAM:DAB
Facsimile: 202.756.8087
Date: November 21, 2006

Please recognize our Customer No. 20277 as our correspondence address.